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RECORD OF ORAL HEARING

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte AKIHIKO KOH, TSUTOMU SAMPEI,
NOBUSHISA WATANABE and AKIHIRO KIKUCHI

Appeal 2009-004407
Application 09/802,857
Technology Center 2100

Oral Hearing Held: May 6, 2010

Before JAMES D. THOMAS, JOSEPH F. RUGGIERO and
MAHSHID D. SAADAT, *Administrative Patent Judges*

ON BEHALF OF THE APPELLANT:

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THE CLERK: Calendar No. 21, Appeal No. 2009-4407. Mr. Dutton?

JUDGE THOMAS: Thank you.

THE CLERK: Mm-hmm.

MR. DUTTON: Yes. We have a guest with me here. It's Ms. Jiyeon Choi. She is a patent agent with our law firm, and has come to observe.

Also, there are some other housekeeping issues --

Okay. I don't know --

JUDGE THOMAS: Have you been to the Board before, sir?

MR. DUTTON: Yes, I have.

JUDGE THOMAS: Okay. So you understand the time limits and --

MR. DUTTON: Yes, I do.

JUDGE THOMAS: Just want to tell you we have a pretty good understanding of the issues on the record.

MR. DUTTON: Okay.

JUDGE THOMAS: And you can proceed on that basis.

MR. DUTTON: Thank you, thank you very much.

I guess before I begin with my opening remarks, I just wanted to ask the Board if there were any specific questions that the Board may have, in order to expedite the process?

If not, then I shall begin.

May it please the Court, my name is Brian Dutton. I am Counsel for Sony Corporation, the Appellant before this Court today.

The following issues before this Court is whether the Examiner the Examiner erred in rejecting the claims in the present application.

We believe that the examples shown within the specification for the present application are indeed commensurate with the scope of the claims.

I would like to first discuss the Sagane reference. That reference, the Examiner appears to have applied that reference as the primary reference in the rejection of the claims on appeal.

Within that reference, there are two particular figures, Figure 1 and Figure 3, which are functional diagrams for the circuitry that the Examiner has relied upon initially.

First starting out with Figure 3 of that reference, because I think that's the easiest figure to discuss presently, if you look at Figure 3 of the Sagane reference, you will notice that there is comparator 8. And that comparator 8 has a signal, some sort of line A that goes to switch 23.

But what you don't see in Figure 3 of Sagane is a signal or some other sort of system that's coming back into the comparator in the form of an interrupt.

And that is one of our features of our claimed inventions, where there is an interrupt that is received by the CPU, and which the process then further advances, once the CPU processes this interrupt.

Now referring to Figure 1 of Sagane, again, we see here that that is a comparator 8, but there is also now an interrupt control circuit 7D.

And then we see some sort of a line that comes from interrupt control 7D, back to the CPU-2. Now the Examiner has identified CPU of Sagane as being the CPU supposedly that would meet our claims.

Now as it turns out, upon a reading of the Sagane reference, there is very little discussion, if any, about what that line is and how it functions with the CPU.

Instead, many of the arguments and discussions about this reference and about this figure refer to the interrupt control circuit, and what the functions of the interrupt control circuit are in handling these instances, where there is some sort of a data match in Element No. 9 of that reference.

So it's our position that the Sagane reference fails to show that the CPU processes -- the CPU-2 -- processes in interrupt, upon receipt of some sort of a coincidence between addresses that may be latched in Element No. 9 of that reference.

Going on to the Suzuki reference, which I believe is probably the next reference that the Examiner has applied, the Examiner has applied that particular reference for the purposes of incrementing and decrementing.

And so the first point of that is that we believe that any other discussion for any other purposes would amount to some sort of a new ground that the Examiner has not put forth in the claims.

But now, one of the things with this Suzuki reference, with this incrementing and decrementing function, is that our claims, specifically in Claim 27, starting out, has a counter-register that is adapted to the store of value, and where the value represents the number of times the interrupt request signal indicates coincidence between the address and the bug address.

That's within our Claim 27, for example.

Now with this Suzuki reference, as we have briefed in our Appeal Brief and our Reply Brief, Figure 2B of this reference you can see in Figure 2B that there is a most significant bit, which has the number of portions of corrected portions.

We believe that that MSB unto itself fails to show how many times this circuitry of Suzuki actually detects the number of coincidences.

All that this MSB circuitry seems to suggest to us is the number of times or the number of corrections that are pre-programmed or downloaded to the system, which is something totally different.

Now of course, the Examiner tries to address that function by saying incrementing and decrementing are one and the same. But again, we do not agree with that position, specifically, the circuitry required to increment and the circuitry required to decrement are not the same circuits.

So of course, with that in mind, I guess in order to increment would require a circuit that's different than what is disclosed within the Suzuki reference.

I guess moving on to Claim No. 40, we have in this particular claim the feature of the counter-reference adopted to store value, the value representing again the number of times.

And again, we've talked about that with the Suzuki reference; and again, wherein the value of the counter is incremented by 1. Again, that was previously discussed.

Moving on to Claim No. 45, this is the claim where there are multiple priority levels. And with this particular feature, I think it was that -- I believe it was the Koscal reference that the Examiner has applied.

And one of the things with this Koscal reference is that that reference fails to show an interrupt. There is no interrupt within the circuit that goes back to the microcontroller or 102.

No interrupt. And if you look at Figure 1, you will not see this interrupt.

Instead, all that this reference does is just merely places different data on a bus. And that's about it. So this reference is not dependent upon the interruption of the microcontroller, but instead, having different data being placed on a data bus for its operating instruction.

And I guess also being a dependent claim this Hosotaini reference, that the Examiner has applied, it appears to operate similar to the Koscal reference, where all that is happening is that a different instruction code is being placed on a bus, on the data bus, as opposed to having the CPU-1 of the Hosotaini reference being interrupted.

And I guess finally, going to Claim No. 52, there are multiple interruptions here that are ended together as a single interrupt.

The Examiner has applied the Hosotaini reference for this particular feature. However, as we can see, looking at this reference, everything coming from the OR gate goes to switches. Switches. Switch 10. None of the outputs from the OR gate 14 goes directly to the CPU. None of it.

So therefore, the Hosotaini reference does not have the circuitry to perform the invention, as we have claimed.

And I guess with that, I ask if there are any specific questions?

JUDGE THOMAS: Any questions from the panel?

JUDGE SAADAT: No questions.

MR. DUTTON: Okay.
With that, I think you very much for your time.
JUDGE THOMAS: Thank you.
Whereupon, at 10:11 a.m., the proceedings were concluded.